Electrónica

Práctica Nº5
Electrónica digital

7 de junio de 2023

1. Objetivos

- Comprobar el funcionamiento de puertas lógicas de dos entradas.
- Implementar una función Booleana usando puertas lógicas.
- Emplear un sumador de cuatro bits para realizar una operación aritmética.
- Comprobar el funcionamiento de un flip-flop tipo JK.

2. Listado de componentes e instrumentos

- Resistencias (1/4 watt): 470 Ω (dos), 1 kΩ y 2,2 kΩ (dos).
- Transistor bipolar BC547 (dos).
- Diodo LED (dos).
- Integrados 74LS00, 74LS02, 74LS83 (o 7483) y CD4027.
- Protoboard.
- Multímetro digital.
- Fuente de tensión de 5 Volts.

3. Puertas lógicas

- Fijar los integrados 74LS00 (puertas NAND) y 74LS02 (puertas NOR) en la protoboard y conectar ambos a la fuente de tensión de 5 Volt. Ver hoja de datos para determinar cuáles son los pines de alimentación.

- Conectando las entradas x e y tanto de una puerta NAND como de otra NOR a los valores lógicos 0 (tierra) y 1 (5 Volt), completar las correspondientes tablas de verdad. Usar el multímetro digital para leer el valor lógico de salida S.

x y	S
0 0	
0 1	
1 0	
1 1	

Cuadro 1: Puerta NAND.

x y	S
0 0	
0 1	
1 0	
1 1	

Cuadro 2: Puerta NOR.

4. Funciones Booleanas

- Armar el circuito combinacional de la Figura 1.

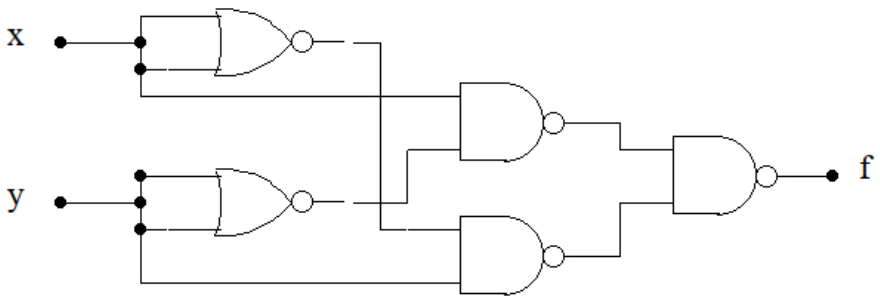


Figura 1: Circuito combinacional.

- Escribir a continuación la expresión algebraica y la tabla de verdad de la función booleana f (salida del circuito combinacional).

$$f =$$

x y	f
0 0	
0 1	
1 0	
1 1	

Cuadro 3: Tabla de verdad de la función f.

- ¿A qué operación binaria de dos entradas típica corresponde esta función booleana?. Para responder a esta pregunta, usar el teorema de De Morgan las veces que sea necesario para reescribir f.

- Conectando las entradas x e y del circuito de la Figura 1 a los valores lógicos 0 (tierra) y 1 (5 Volt), medir la tabla de verdad de f.

x	y	f
0	0	
0	1	
1	0	
1	1	

Cuadro 4: Tabla de verdad medida de la función f.

5. Sumador binario de 4 bits

- Fijar el integrado 74LS83 (sumador binario de 4 bits) en la protoboard. Guiándose por el diagrama de pines dado en la hoja de datos, conectar la tierra (pin 12) y la alimentación de 5 Volt (pin 5).

- Leyendo la hoja de datos, determinar qué pines corresponden a los 4 bits de cada uno de los dos números de entrada, (A_3, A_2, A_1, A_0) y (B_3, B_2, B_1, B_0), a los acarreos de entrada y salida, C_0 y C_4, y a la suma (S_3, S_2, S_1, S_0).

- Usar el integrado para realizar la suma binaria $(1010)_2 + (0111)_2$. Comprobar que tanto la suma como el acarreo de salida son correctos. Dibujar a continuación el esquema de conexiones usado.

6. Flip-flops

- Fijar el integrado CD4027 (flip-flop tipo JK dual) en la protoboard y conectar los pines V_{SS} a tierra y V_{DD} a la tensión de 5 Volt. Ver la hoja de datos para identificar cuáles son estos pines.

- Armar el circuito de la Figura 2 usando uno de los dos flip-flop del integrado 4027. Para que quede habilitado, las correspondientes entradas directas SET y RESET deben conectarse a tierra (ver tabla de verdad en la hoja de datos).

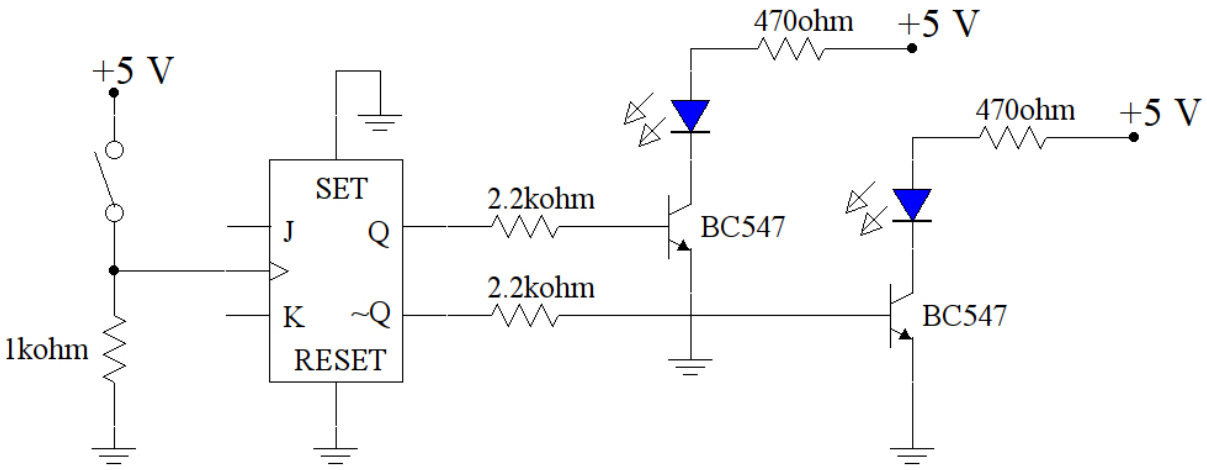


Figura 2: Flip-flop tipo JK.

- Conectando las entradas J y K a los valores lógicos 0 (tierra) y 1 (5 Volt), completar la tablas de verdad del Cuadro 5. Usar el switch para emular una señal de clock que dispara al integrado por flanco positivo.

J K	Q Q'
0 0	
0 1	
1 0	
1 1	

Cuadro 5: Tabla de verdad del flip-flop JK.

- Por último, conectando ambas entradas J y K al valor lógico 1 y generando varios pulsos de clock, verificar que el flip-flop JK bascula su salida.

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS00
Quad 2-Input NAND Gate

General Description

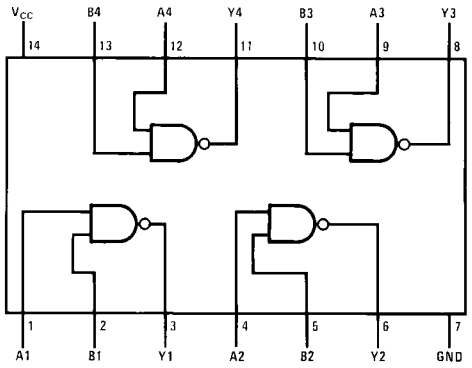
This device contains four independent gates each of which performs the logic NAND function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS00M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS00SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS00N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		0.8	1.6	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.4	4.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

FAIRCHILD SEMICONDUCTOR™

May 1986
Revised March 2000

DM74LS02
Quad 2-Input NOR Gate

General Description

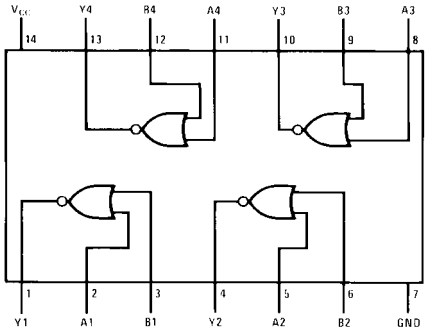
This device contains four independent gates each of which performs the logic NOR function.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS02M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS02SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS02N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max		1.6	3.2	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max		2.8	5.4	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

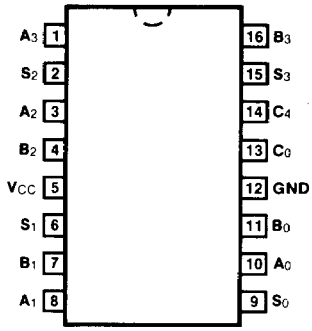
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output		13		18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output		10		15	ns

54/7483A
54LS/74LS83A

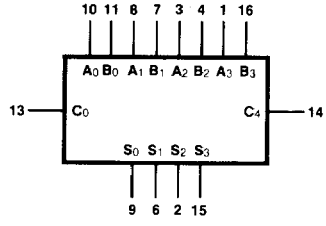
4-BIT BINARY FULL ADDER
(With Fast Carry)

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '83A high speed 4-bit binary full adders with internal carry lookahead accept two 4-bit binary words ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). They generate the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. They operate with either HIGH or active LOW operands (positive or negative logic). The '283 is recommended for new designs since it features standard corner power pins.

LOGIC SYMBOL



VCC = Pin 5
GND = Pin 12

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	7483APC, 74LS83APC		9B
Ceramic DIP (D)	A	7483ADC, 74LS83ADC	5483ADM, 54LS83ADM	6B
Flatpak (F)	A	7483AFC, 74LS83AFC	5483AFM, 54LS83AFM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	A Operand Inputs	1.0/1.0	1.0/0.5
$B_0 - B_3$	B Operand Inputs	1.0/1.0	1.0/0.5
C_0	Carry Input	1.0/1.0	0.5/0.25
$S_0 - S_3$	Sum Outputs	20/10	10/5.0 (2.5)
C_4	Carry Output	10/5.0	10/5.0 (2.5)

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 2004

CD4027BC
Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

The CD4027BC dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

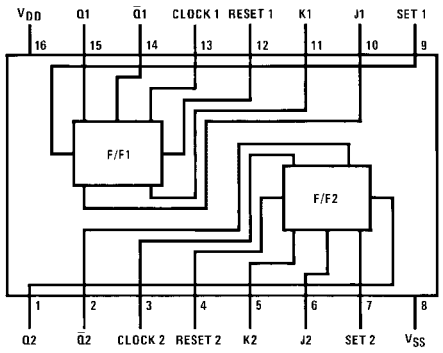
Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Low power: 50 nW (typ.)
- Medium speed operation: 12 MHz (typ.) with 10V supply

Ordering Code:

Order Number	Package Number	Package Description
CD4027BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4027BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Top View

Truth Table

Inputs t_{n-1} (Note 1)						Outputs t_n (Note 2)	
CL (Note 3)	J	K	S	R	Q	Q	$\overline{Q}$
↗	I	X	O	O	O	I	O
↗	X	O	O	O	I	I	O
↗	O	X	O	O	O	O	I
↗	X	I	O	O	I	O	I
↘	X	X	O	O	X		(No Change)
X	X	X	I	O	X	I	O
X	X	X	O	I	X	O	I
X	X	X	I	I	X	I	I

I = HIGH Level
O = LOW Level
X = Don't Care
↗ = LOW-to-HIGH
↘ = HIGH-to-LOW

Note 1: t_{n-1} refers to the time interval prior to the positive clock pulse transition

Note 2: t_n refers to the time intervals after the positive clock pulse transition

Note 3: Level Change

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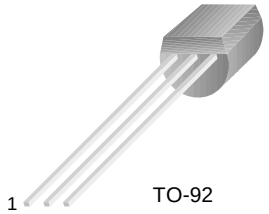
SEMICONDUCTOR®

BC546/547/548/549/550

Switching and Applications

- High Voltage: BC546, V_{CEO}=65V
- Low Noise: BC549, BC550
- Complement to BC556 ... BC560



TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage : BC546	80	V
	: BC547/550	50	V
	: BC548/549	30	V
V_{CEO}	Collector-Emitter Voltage : BC546	65	V
	: BC547/550	45	V
	: BC548/549	30	V
V_{EBO}	Emitter-Base Voltage : BC546/547	6	V
	: BC548/549/550	5	V
I_C	Collector Current (DC)	100	mA
P_C	Collector Power Dissipation	500	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{CBO}	Collector Cut-off Current	V_{CB}=30V, I_E=0			15	nA
h_{FE}	DC Current Gain	V_{CE}=5V, I_C=2mA	110		800	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		90	250	mV
		I_C=100mA, I_B=5mA		200	600	mV
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C=10mA, I_B=0.5mA		700		mV
		I_C=100mA, I_B=5mA		900		mV
V_{BE} (on)	Base-Emitter On Voltage	V_{CE}=5V, I_C=2mA	580	660	700	mV
		V_{CE}=5V, I_C=10mA			720	mV
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=100MHz		300		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		3.5	6	pF
C_{ib}	Input Capacitance	V_{EB}=0.5V, I_C=0, f=1MHz		9		pF
NF	Noise Figure : BC546/547/548	V_{CE}=5V, I_C=200μA		2	10	dB
	: BC549/550	f=1KHz, R_G=2KΩ		1.2	4	dB
	: BC549	V_{CE}=5V, I_C=200μA		1.4	4	dB
	: BC550	R_G=2KΩ, f=30~15000MHz		1.4	3	dB

h_{FE} Classification

Classification	A	B	C
h_{FE}	110 ~ 220	200 ~ 450	420 ~ 800